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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,196	03/25/2004	Brian Holscher	TRAN-P247	8666

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EXAMINER	
GU, SHAWN X	
ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/18/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/810,196	HOLSCHER ET AL.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 October 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office action is in response to the amendment filed on 11 October 2006. Claims 1-20 are pending. All objections and rejections not repeated below are withdrawn.

Claim Objections

2. Claims 2-4 are objected to because of the following informalities:

Per claim 2, on line 2, the term "an accesses" contains grammatical or typographical errors. It should be changed to "accesses".

All dependent claims are objected to as having the same deficiencies as the claims they depend from. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-15, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno et al. [US 6,678,795 B1] (hereinafter "Moreno").

Per claims 1, 9, and 18, Moreno teaches a request tracking data prefetch apparatus (Fig 2, combination of 204 Li, 254 Lj, 206 CCi, 256 CCj, 282 PUM Table, 284 Prefetch Engine) for a computer system (the system in Fig 2), comprising:

a processor (Fig 2, 252 Pj);

a system memory (Fig 2, 270 Memory) coupled to the processor;

a prefetch unit (Fig 2, combination of 290 PUM Engine and 256 CCj; Col 5, Lines 56-58) coupled to the system memory;

a plurality of trackers (PUM Entries; Col 4, Lines 45-57) included in the prefetch unit, wherein the trackers are respectively configured to recognize an access to a plurality of cache lines and accesses to pages of the system memory by a processor of the computer system (Col 4, Lines 45-57; Col 5, Lines 58-67; Col 7, Lines 1-7; also presented by the rows of Fig 1's table); and

a cache memory (Fig 2, 254 Lj) coupled to the prefetch unit, wherein the prefetch unit uses a bit vector (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) to predictively load target cache lines from the system memory into the cache memory (Col 4, Lines 58-67; Col 5, Lines 1-2) to reduce an access latency of the processor (Col 4, Lines 36-44), and wherein the target cache lines are indicated by the trackers (Col 7, Lines 4-10 and Lines 28-63).

Although Moreno does not clearly state that the accesses to the plurality of cache lines form a stream type access pattern, the reference does imply that Moreno's teaching is configured to pre-fetch cache lines based on a stream type access pattern (Moreno is not limited to only pre-fetch based on sequential pattern, which indicates that Moreno is capable of doing that and more, see Col.1, Ln.63-67 and Col.2, Ln.1-2). To illustrate, it is understood that a stream type access pattern is formed by non-repeated sequential accesses to a group of adjacent or sequential cache lines, and it would have been obvious to one ordinarily skilled in the art that the row entry with Index 1502688 in Figure 1 could be one of such stream type access pattern formed by previous sequential cache line accesses. The total number of accesses for this row is two for the total of two cache lines accessed (the lines marked with "1"), which implies that each cache line is accessed only once previously. This could be a stream type access pattern as the two cache lines are adjacent to each other, with each accessed once. Then, according to the pre-fetch technique taught by Moreno (see Col.6, Ln.56-67 and Col.7, Ln.1-3), when a new access hit one of the two cache lines (the one with the lower address), the other cache line with the higher adjacent address would be pre-fetched. Moreno does not specifically disclose that the order of previous accesses to the two cache lines was not interrupted by other cache line accesses. However, in the case that the pattern was created by a stream type access to the two adjacent cache lines, the accesses must be sequential in order if those two lines contained stream data. Another entry with the Index 183965 in Figure 1 shows a similar and more elaborate example of a possible stream type access pattern, with 32 adjacent cache lines each

accessed only once previously. This could be the result of accessing a longer block of stream type data. The cache line access patterns exhibited in Moreno's Figure 1 are for illustration purposes only and are not the only possible patterns recognized by Moreno's system, and it would be obvious to one ordinarily skilled in the art that any type of cache line access patterns can be recognized by Moreno's PUM entries, including stream type access pattern. Stream type access pattern is the result of accessing stream type data, which is one of many possible types of data stored on Moreno's computer system.

Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Moreno is configured to recognize a stream type access pattern (by searching and identifying the cache lines with their corresponding bits set to "1" in the PUM entry, see Col.6, Ln.56-67 and Col.7, Ln.1-3) and predicatively load a target cache line indicated by the stream-type access pattern (the explanation set forth above clear describes this, also see "prefetch based on sequential pattern", in col.1, ln.63-67).

It is clear claim 1's apparatus for a computer system is already described by the apparatus of claim 9, and the high latency memory and low latency memory of claim 1 respectively correspond to the system memory and cache memory of claim 9.

It is also clear that the method of claim 18 is performed by the apparatus of claim 9, as the bit vector of claim 9 clearly tracks multiple data transfer patterns (as clearly indicated by the cache line access history patterns displayed by the rows of Fig 1) between the high latency memory/system memory and the lower latency memory/cache memory.

Per claims 2 and 10, Moreno further teaches each of the trackers include a tag (PUM entry bits that indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) configured to recognize accesses to corresponding cache lines of the high latency memory by the processor.

Per claims 3 and 11, Moreno further teaches a plurality of system memory accesses by the processor to the high latency memory as recognized by the tag are used by the trackers to determine the target cache line for a predictive load into the cache memory/low latency memory (Col 7, Lines 4-10 and Lines 28-63).

Per claims 4, 12, and 20, Moreno further teaches accesses by the processor to adjacent cache lines of a page (Fig 1, rows with adjacent "1"s) of the system memory are used to determined the target cache line of a stream type access pattern for a predictive load into the cache memory, wherein the adjacent cache lines have adjacent addresses (Col 4, Lines 45-57; Col 5, Lines 3-22; Col 7, Lines 4-10 and Lines 28-63).

Moreno does not specifically teach that these accesses are consecutive. However, in Moreno's Fig 1, rows with Indexes 184772, 1502531, 1502688 all indicate 2 or 3 total page accesses to a page with only 2 adjacent cache lines indicated as accessed, and it would have been obvious to one ordinarily skilled in the art at the time of the Applicant invention that objects or programs bigger than a cache line (128 bytes) are stored in more than one adjacent cache lines of the same page, and when they are requested by the processor, these cache lines will be accessed consecutively by the processor. For instance, if an object between the size of 129 bytes and 256 bytes is stored in the page with index 184772, then a request by the processor for this object would result in consecutive accesses to the two adjacent cache lines storing the object, and these accesses are used by Moreno's invention to determine the target cache line for a predictive load into the cache memory. Furthermore, Moreno also teaches these accesses are consecutive as set forth above in claims 1, 9 and 18 (stream type cache line access pattern).

Per claim 5, Moreno further teaches the high latency memory comprises a memory block of a plurality of memory blocks of the computer system (pages; Col 4, Lines 36-44).

Per claims 6 and 13, Moreno further teaches the system/high latency memory comprises a plurality of 4KB pages (Col 4, Lines 36-44; Col 5, Lines 11-14), and the memory block comprises a four kilobyte page (a memory block is a 4KB page).

Per claims 7 and 14, Moreno further teaches each of the plurality of trackers includes a tag configured to monitor a sub portion of the high latency memory block/page for accesses by the processor (a portion of the PUM entry bits which indicate cache line accesses of a page, in other words; Col 4, Lines 45-57; Col 5, Lines 3-22; since access to every cache line of a page is represented by a corresponding bit in the PUM entry, a portion of those bits monitor a sub portion of a page for accesses).

Per claim 8, Moreno further teaches the high latency memory is a system memory (Fig 2, 270 Memory; Col 5, Lines 36-55; Memory 270 is main memory of computer system 200) of the computer system.

Per claim 15, Moreno further teaches the cache lines 128 byte cache lines (Col 5, Lines 12-14) and wherein a tag (half of the PUM entry bits which indicate cache line accesses of a page; Col 4, Lines 45-57; Col 5, Lines 3-22) is used to monitor half of a page (since access to every cache line of a page is represented by a corresponding bit in the PUM entry, half of those bits monitor half of a page) for accesses by the processor.

5. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Bittel et al. [US 6,820,173 B1] (hereinafter "Bittel").

Per claim 16, Moreno already substantially discloses the claim as described above, but does not specifically disclose that the cache memory is a prefetch cache memory within the prefetch unit. However, Bittel teaches a prefetch apparatus (Fig 7) comprising a prefetch unit (Fig 3, 208 Prefetcher), and a cache memory (Fig 3, 306 Cache) within the prefetch unit. It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to include Bittel's cache memory in Moreno's prefetch unit in order to further increase caching capacity of the system while allow the existing caches (L1, L2, etc) to serve their original purposes, furthermore by using an internal cache of the prefetcher instead of the L1 cache, there is no additional interconnection wiring required between the prefetcher and the L1 cache.

6. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Microsoft Computer Dictionary (hereinafter "Microsoft").

Per claim 17, Moreno already substantially discloses the claim as described above, and further teaches the cache memory is an L1 cache memory (Col 5, Lines 12-13), but does not specifically disclose that the cache memory is an L2 cache memory. However, Microsoft discloses that a typical L2 cache has bigger capacity than a typical L1 (Page 304), and therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make Moreno's cache memory a L2 cache instead of a L1 cache in order to have larger caching capacity.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Moreno [US 6,678,795 B1], further in view of Brooks [6,081,868] (hereinafter "Brooks").

Per claim 19, Moreno already substantially discloses the claim as described above, and further teaches the computer system includes a plurality of processors (Fig 2, 202 Pi and 252 Pj), and wherein each of the processors is coupled to a respective lower latency memory (Fig 2, 204 Li and 254 Lj) and are all coupled to a high latency memory (Fig 2, 270 Memory), but does not specifically disclose that each of the processors is coupled to a respective high latency memory. However, Brooks teaches a prefetch system wherein each of a plurality of processors is coupled to a respective

high latency memory (Brooks: Fig 2, a CPU is coupled to a CPU private memory in each CPU block; CPU Private Memory has higher latency than CPU Cache), in order to provide data storage exclusively for the associated CPU (Brooks: Col 5, Lines 25-30). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to make each of Moreno's plurality of processors to be coupled to a respective high latency memory in order to provide data storage exclusively for the associated processor.

Response to Arguments

8. Applicant's arguments with respect to the amended claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. The newly added limitations are taught by the previously cited references Moreno [US 6,678,795 B1], Bittel [US 6,820,173 B1], Microsoft and Brooks [6,081,868] as set forth above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

9 November 2006

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